

THE DESIGN OF A NEW SIGNAL PROCESSING SUBSYSTEM FOR THE WSR-88D (NEXRAD) RADAR

A PROJECT LEADING TO

**REPLACEMENT OF THE SIGNAL PROCESSING
SUBSYSTEM (SPS) AND THE STATUS AND
CONTROL COMPUTER (RDASC) IN THE WSR-88D
RADAR DATA ACQUISITION (RDA) FUNCTIONAL
AREA**



A PREREQUISITE FOR

- **NEW FEATURES, I.E. POLARIMETRY**
- **PERFORMANCE ENHANCEMENT**
- **REDUCING IMPACT OF OBSOLESCENCE**

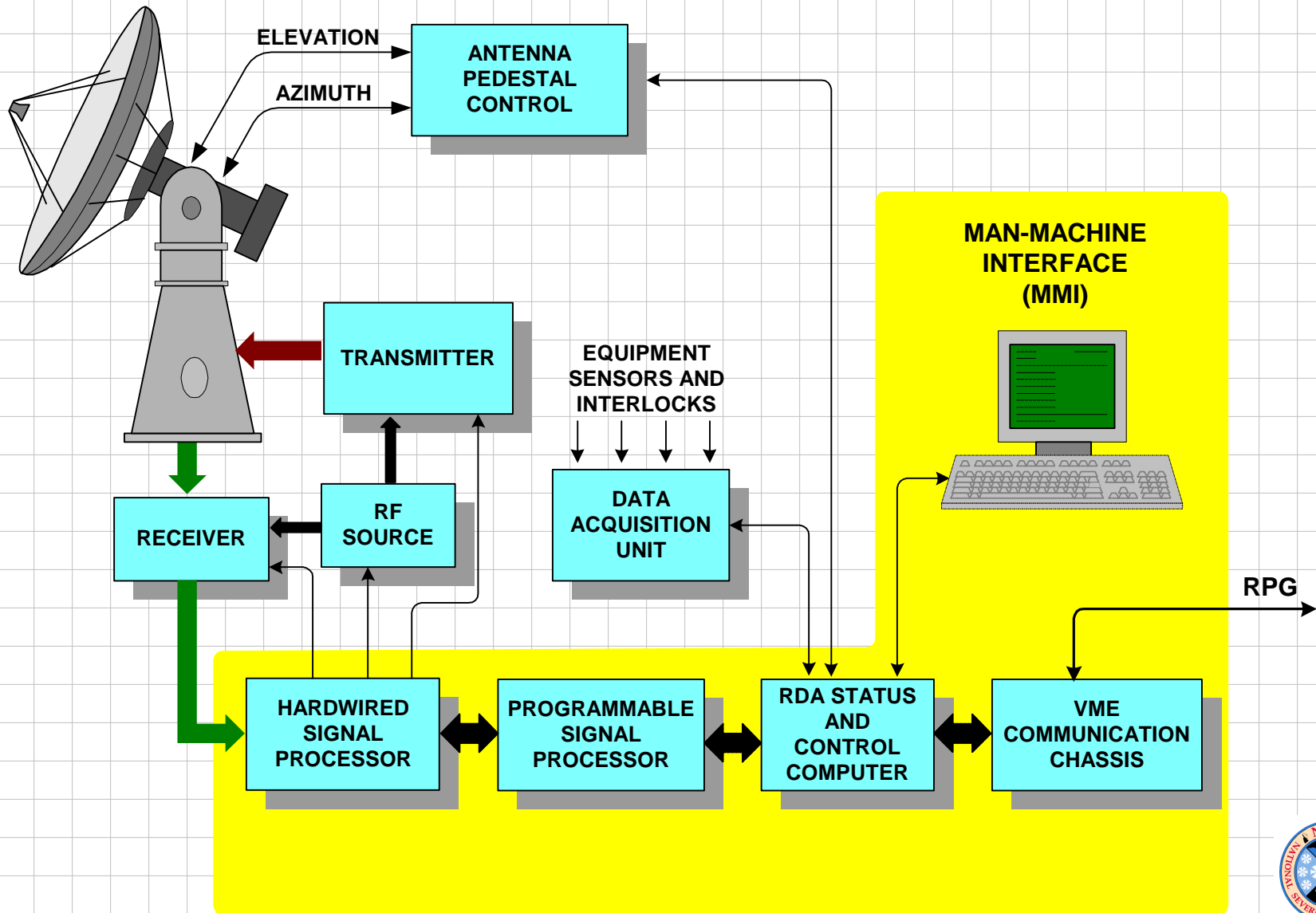


CHARACTERISTICS

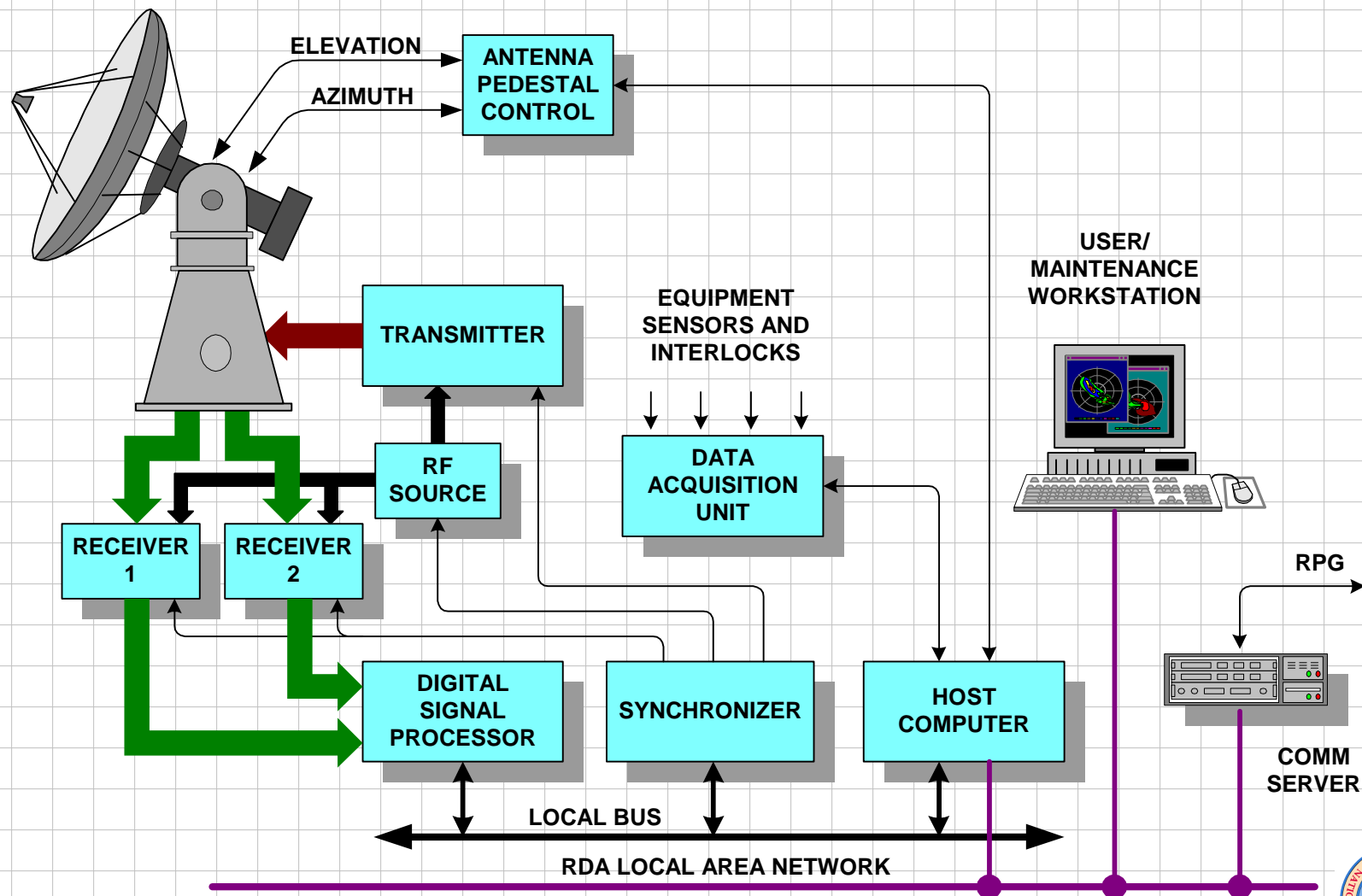
- **MODULAR**
- **SCALEABLE**
- **OPEN SYSTEM STANDARDS**
- **COTS**



EXISTING RDA CONFIGURATION



PROPOSED RDA CONFIGURATION

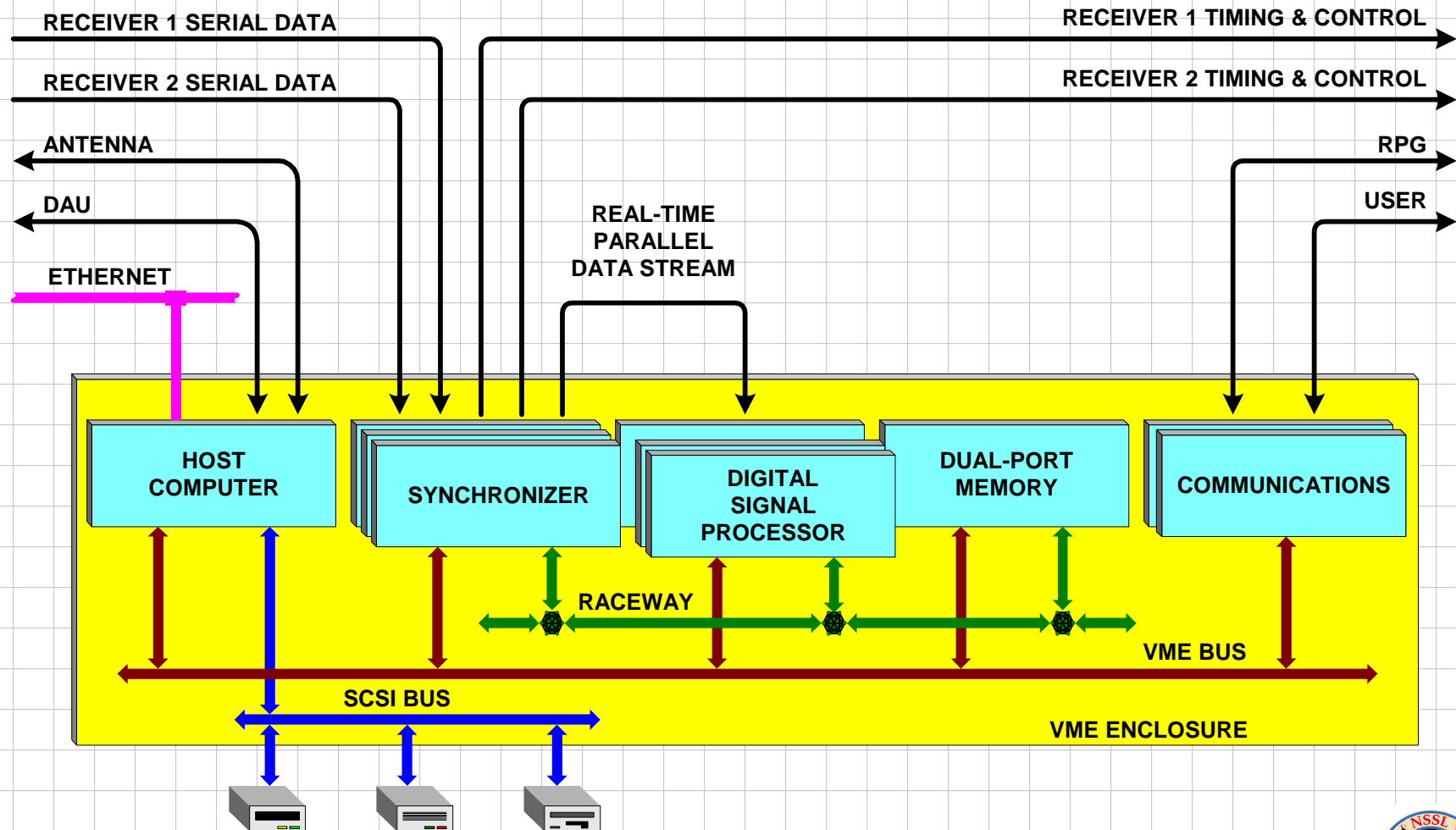


PROTOTYPE CHARACTERISTICS

- **STANDARD VME-64 ARCHITECTURE**
- **STANDARD 6U FORM FACTOR**
- **INTEGRATED COTS SINGLE BOARD HOST COMPUTER**
- **INTEGRATED COTS SIGNAL PROCESSOR SUBSYSTEM**
- **CUSTOM IN-HOUSE DESIGNED SYNCHRONIZER AND CONTROL SUBSYSTEM**
- **MULTI-TASKING POSIX COMPLIANT REAL-TIME OPERATING SYSTEM**



HARDWARE PLATFORM



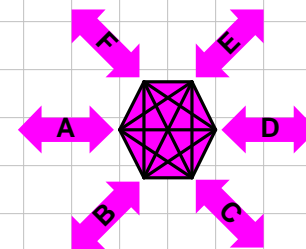
DIGITAL SIGNAL PROCESSOR

- **HETEROGENEOUS MULTICOMPUTER SYSTEM DEVELOPED BY MERCURY COMPUTER SYSTEMS INC.**
- **BASED ON INDUSTRY STANDARD RACEWAY SWITCHED INTERCONNECT FABRIC**
- **USING FAST 6-PORT CROSSBAR SWITCH TECHNOLOGY**
- **FEATURES EXTREMELY HIGH BANDWIDTH DATA TRANSFER**
- **USES SUPER HARVARD ARCHITECTURE (SHARC) DSP FROM ANALOG DEVICES**
- **EASILY EXPANDABLE TO SEVERAL HUNDRED PROCESSORS**

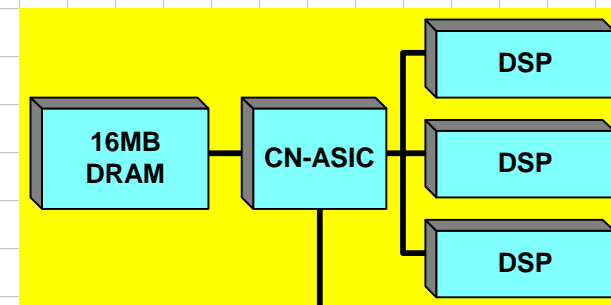


SIGNAL PROCESSOR COMPONENTS

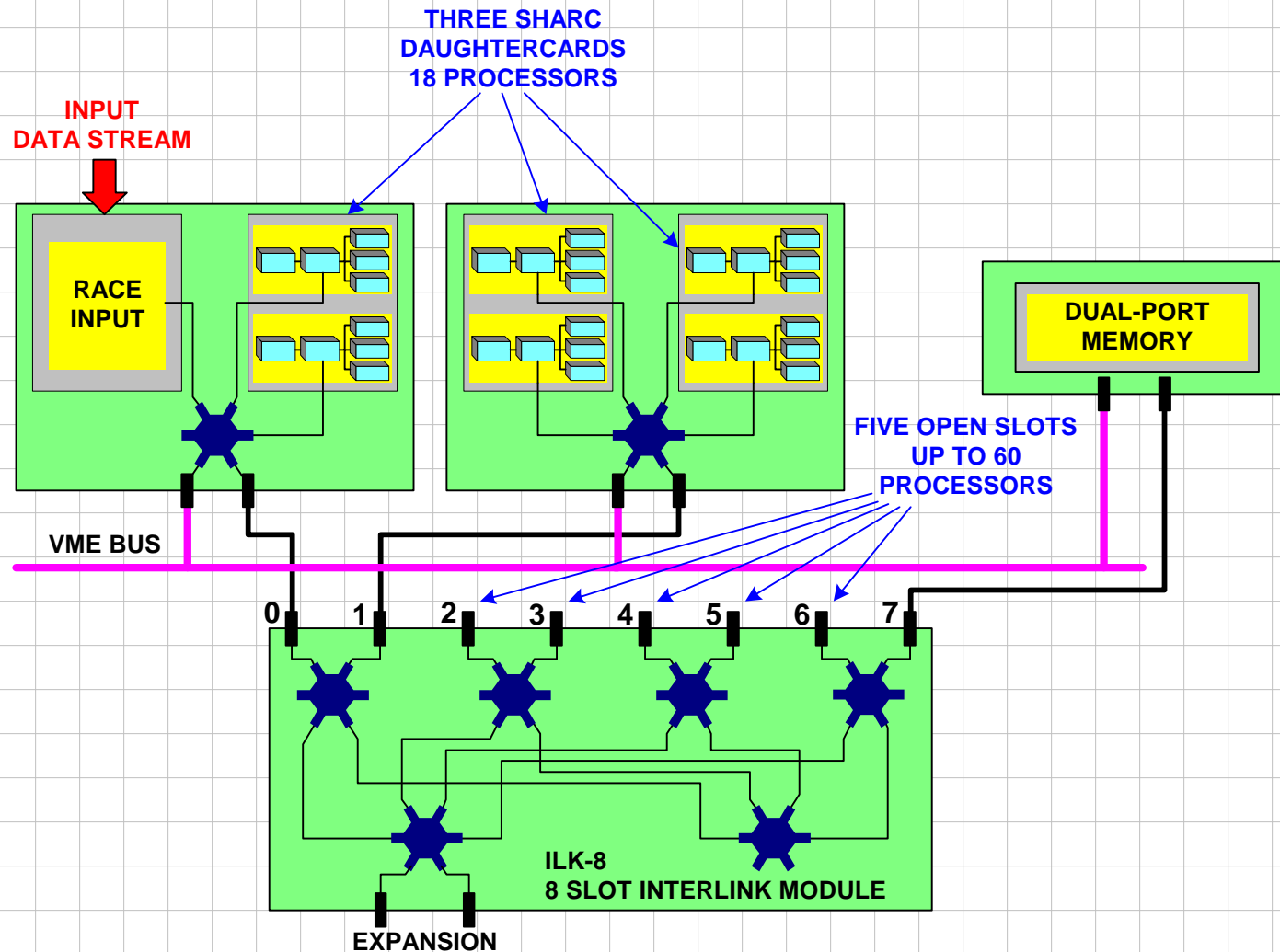
**HIGH-SPEED 6-PORT
CROSSBAR SWITCH ALLOWS
MULTIPLE TRANSACTIONS
WITH MINIMUM LATENCY**



**HETEROGENEOUS COMPUTE
NODES CAN BE DIFFERENT
TYPES OF PROCESSOR,
MEMORY OR I/O PORTS**

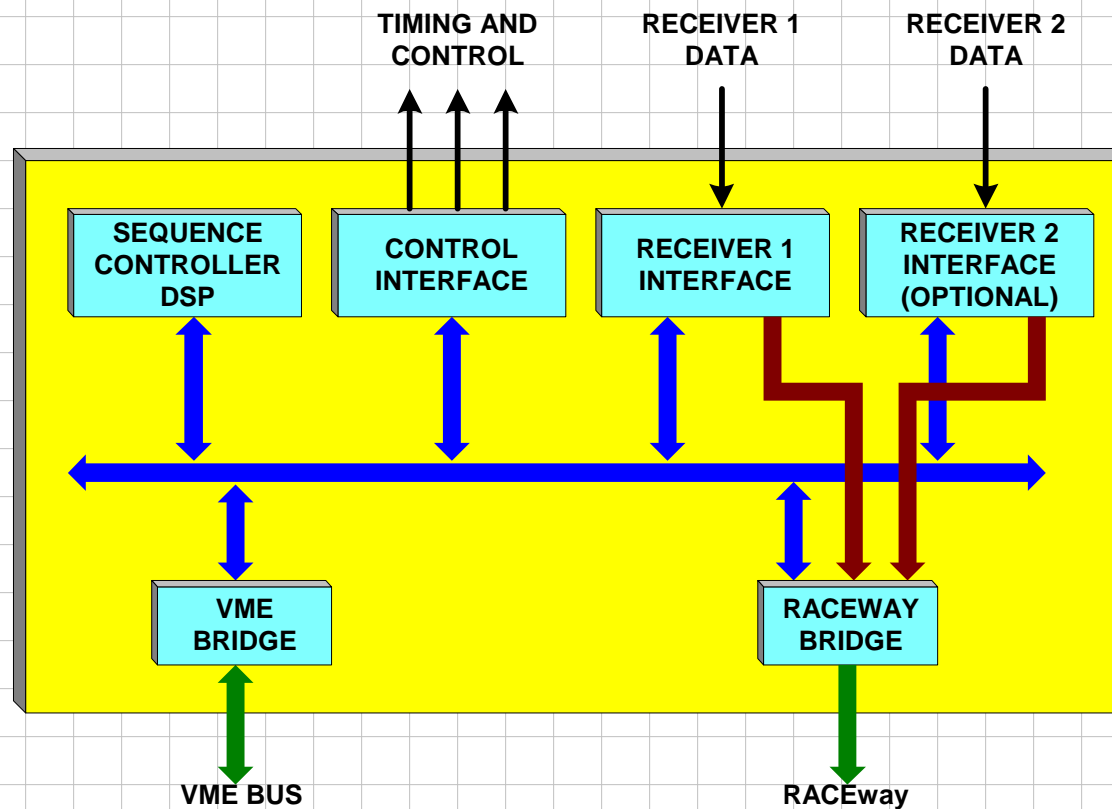


HARDWARE CONFIGURATION



RADAR TIMING AND CONTROL

CUSTOM DESIGNED SYNCHRONIZER BASED ON A HIGH-SPEED PROGRAMMABLE SEQUENCER



DEVELOPMENT ENVIRONMENT

DISTRIBUTED DEVELOPMENT AND TESTING USING ACTUAL TARGET PLATFORMS

